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# A HYBRID APPROXIMATE MULTIPLIER FOR ENERGY EFFICIENT IMAGE PROCESSING

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## ABSTRACT

This paper explores the realm of Very Large-Scale Integration (VLSI) circuits, energy-efficient and low-power solutions are critical for modern applications. This paper presents a novel 8-bit Hybrid Approximate Vedic Multiplier (HAVM) designed to address the high-power consumption and extensive hardware requirements typically associated with multiplication operations in image processing applications. Utilizing the "Urdhva Tiryagbhyam" sutra from Vedic Mathematics, the HAVM is based on the Vertical and Crosswise technique, which accelerates computation and reduces complexity. By strategically introducing approximations, the proposed design minimizes both power and area usage without significantly compromising accuracy, making it ideal for real-time image processing tasks. The Xilinx Vivado Design Suite was employed for synthesis and simulation, while Verilog was used for hardware implementation. Compared to traditional precise multipliers, the HAVM achieves substantial reductions in energy consumption and hardware footprint, showcasing the relevance of approximate computing in achieving optimized performance for energy- efficient device designs.

## INTRODUCTION

Multipliers play a crucial role in microprocessors, digital signal processing (DSP) circuits, and various communication technologies. Traditional multiplication techniques require a significant number of adders to compute partial products, leading to increased hardware complexity, power consumption, and latency. As the demand for high-speed and energy-efficient processors grows, alternative multiplication methods have gained attention.

Vedic mathematics, an ancient Indian mathematical system, offers efficient computational techniques based on 16 fundamental sutras (formulas). One of these sutras, Urdhva Tiryagbhyam, provides a unique approach to multiplication that enables faster calculations with reduced hardware requirements. Leveraging this technique, approximate multipliers can be developed to optimize performance for specific applications, particularly in image processing, where minor errors are often tolerable.

This project introduces an 8×8 Hybrid Approximate Vedic Multiplier (HAVM), which integrates Vedic multiplication principles with approximation techniques. The primary objective is to achieve a balance between computational accuracy, power efficiency, and hardware optimization. The proposed HAVM employs NAND-based Approximate Half Adders (NHA) to minimize power consumption while maintaining acceptable

computational accuracy. Unlike traditional multipliers, this hybrid approach reduces complexity by selectively processing only significant portions of input data, thereby lowering circuit area and energy usage.

The implementation of the HAVM is carried out using Verilog HDL and simulated using the Xilinx Vivado Design Suite. The design is further synthesized on a Zed Board Zynq- 7000 SoC to evaluate its real-time performance. Comparative analysis with conventional multipliers demonstrates that the HAVM achieves notable reductions in power and latency, making it highly suitable for energy-efficient applications such as image and audio processing.

## LITERATURE SURVEY

- **Title:** "Design of 4x4 Bit Vedic Multiplier Using EDA Tool"

  **Description:** This study explores the efficiency of Vedic multipliers, particularly using the Urdhva Tiryagbhyam sutra. It demonstrates improved computational speed and area reduction compared to conventional multiplication techniques. However, it does not focus on power efficiency or approximation strategies. Year of Publication: 2012.

- **Title:** "Design and Implementation of 8-Bit Vedic Multiplier"

  **Description:** This research extends the Vedic multiplier to an 8-bit design, showcasing the benefits of carry-skip adders for partial product addition. While it enhances speed and area utilization, it does not employ approximation techniques to further optimize power consumption. Year of Publication: 2013.

- **Title:** "Energy Efficient Approximate 8-Bit Vedic Multiplier"

  **Description:** This study introduces approximate computing principles in Vedic multiplication to reduce power consumption. It strategically omits less significant bits, leading to minor computational errors while achieving significant energy savings. However, it does not explore hybrid approaches combining multiple multiplier architectures. Year of Publication: 2022.

- **Title:** "Implementation of an Efficient N×N Multiplier Based on Vedic Mathematics and Booth-Wallace Tree Multiplier"

  **Description:** This research integrates Vedic, Booth, and Wallace-tree multiplication algorithms, leveraging their strengths to optimize speed and area efficiency. While it reduces latency, it does not incorporate approximate adders to minimize power consumption further. Year of Publication: 2019.

- **Title:** "High-Performance Approximate Half and Full Adder Cells Using NAND Logic Gates"

  **Description:** This paper investigates NAND-based Approximate Half Adders (NHA), which enhance speed and reduce power usage in arithmetic circuits. The methodology is applied to approximate multipliers, but the study lacks an in-depth analysis of its impact on real-world FPGA implementations. Year of Publication: 2019.

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## PROPOSED SYSTEM

**A. 4×4 Bit Approximate Multiplier (AVM):** The 4-bit operands are divided into upper and lower halves by the algorithm. These segments are then multiplied, including the cross products. To obtain the final output, the results are combined in the subsequent addition step, and any necessary carry propagation is carried out. In the implementation of the 4-bit Approximate Multiplier (AVM), the 2-bit AVM serves as the foundation. Figure 4 illustrates the understanding of this module. As shown in the figure, four 2- bit AVM modules are used in the design of the 4-bit AVM. The addition operation of two 4-bit operands is handled by a 4-bit ripple carry adder. This is achieved through the coordinated operation of four full adders.

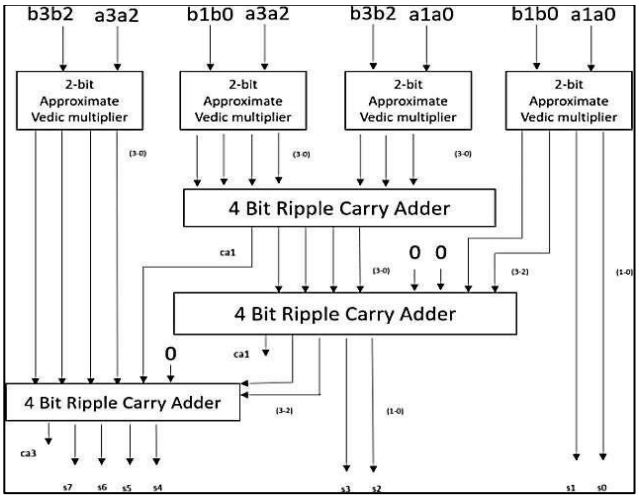


Figure.1 4×4 Bit Approximate Multiplier

**B. 8×8 bit Hybrid Approximate Vedic Multiplier:** The multiplier leverages Vedic algorithms, which simplify multiplication by breaking it down into smaller, more manageable sub-processes. This method can lead to faster computation compared to traditional multiplication approaches. The design of the 8-bit Vedic multiplier (VM) involves utilizing four 4-bit VMs along with adder circuits. The output of this 8-bit VM is accurate, consumes a reasonable amount of energy, and experiences reduced delay

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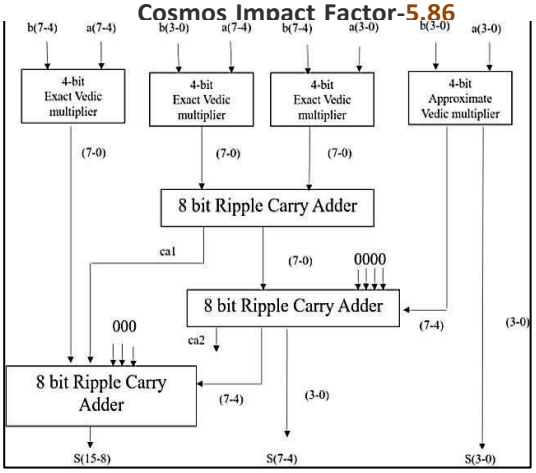


Figure.2 8×8-bit Hybrid Approximate Vedic Multiplier

The proposed 8×8 HAVM design includes three 4-bit VM modules and one 4-bit Approximate Vedic Multiplier (AVM) module. The use of the 4-bit AVM on the least significant bits introduces some permissible errors in the output. However, this approximation method, along with the hybrid design, results in a simpler circuit, requiring fewer gates and consuming less power. The reduced complexity leads to more compact designs, potentially saving significant chip area.

## SIMULATION RESULTS

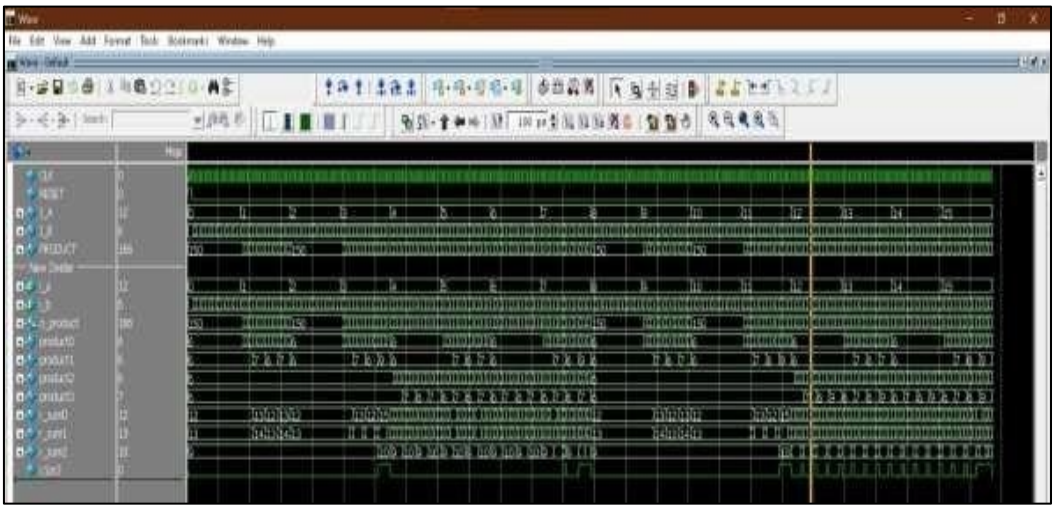

Figure.3 4x4 AVM output



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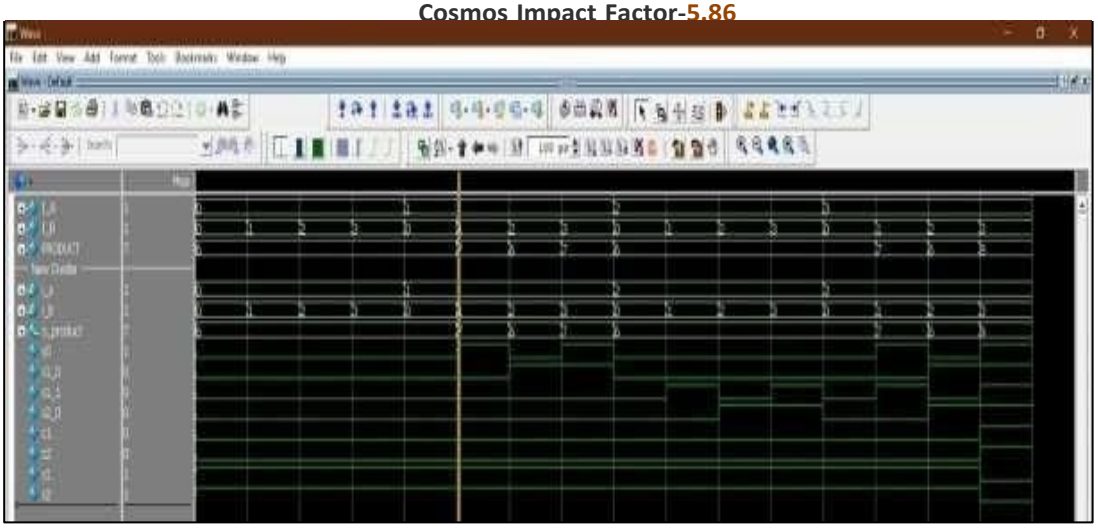

Figure.4 2x2 AVM output

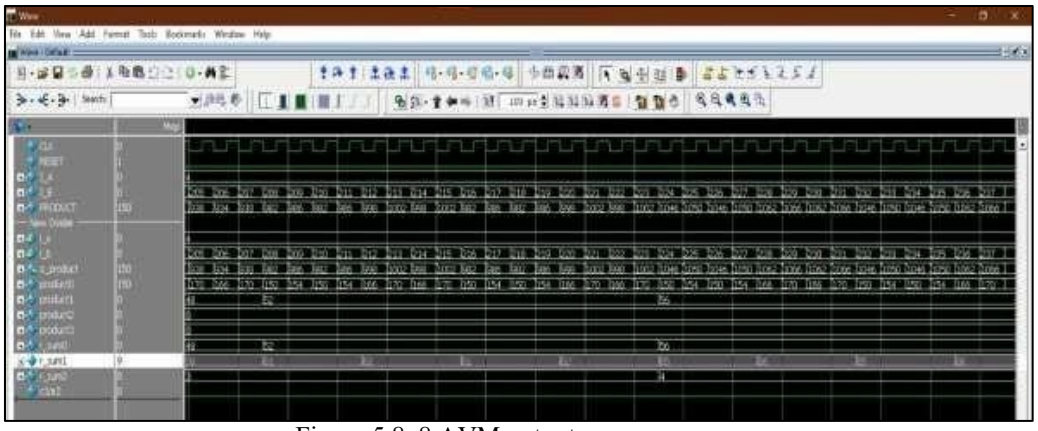

Figure.5 8x8 AVM output

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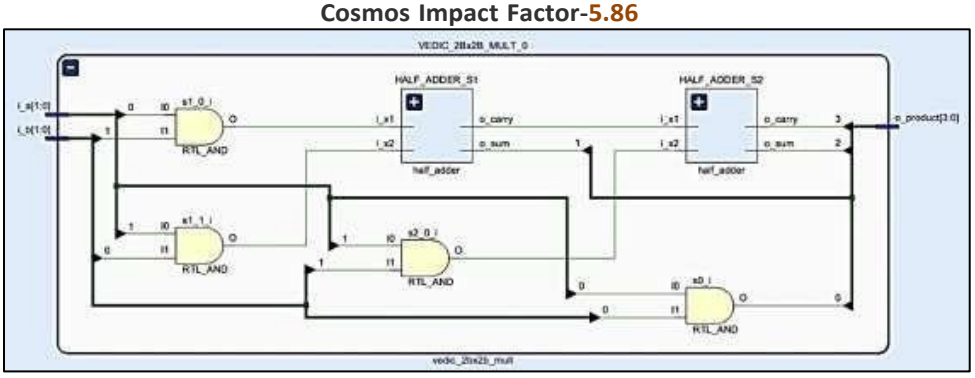


Figure.6 RTL Schematic Exact 2x2 Vedic Multiplier

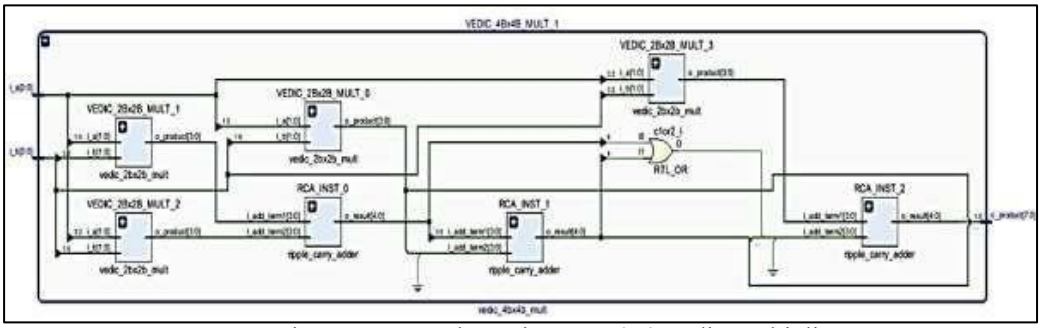


Figure.7 RTL Schematic Exact 4x4 Vedic Multiplier

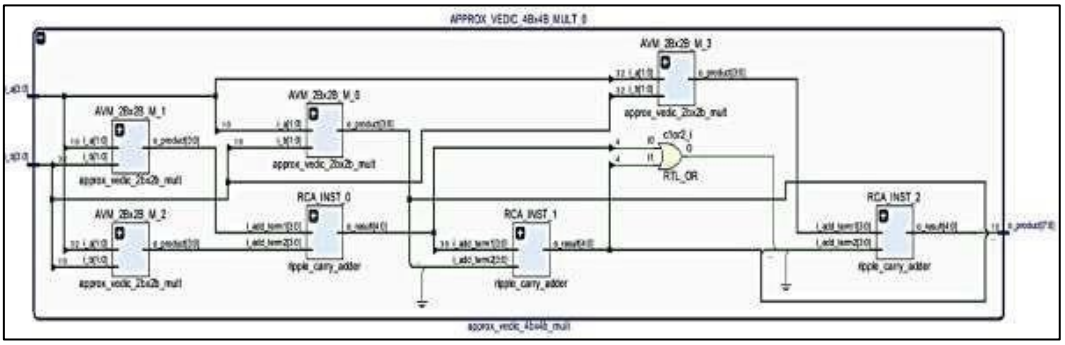


Figure.8 RTL Schematic Exact 4x4 Approx Vedic Multiplier

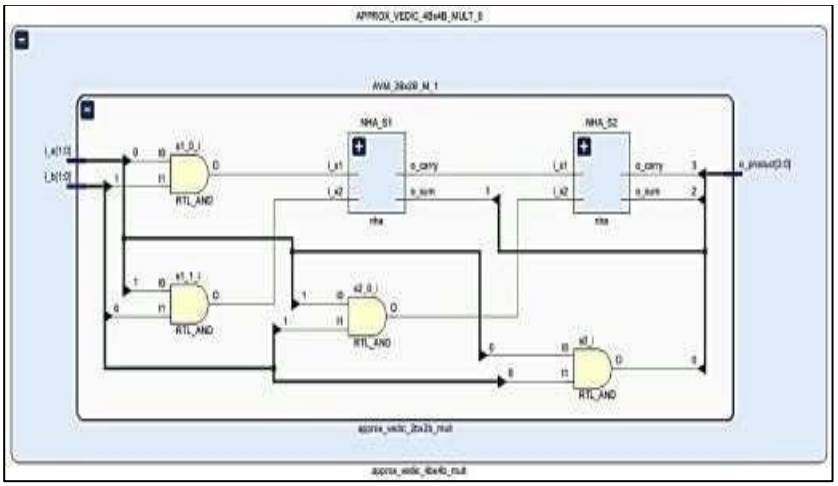


Figure.9 RTL Schematic Exact 2x2 Approx Vedic Multiplier

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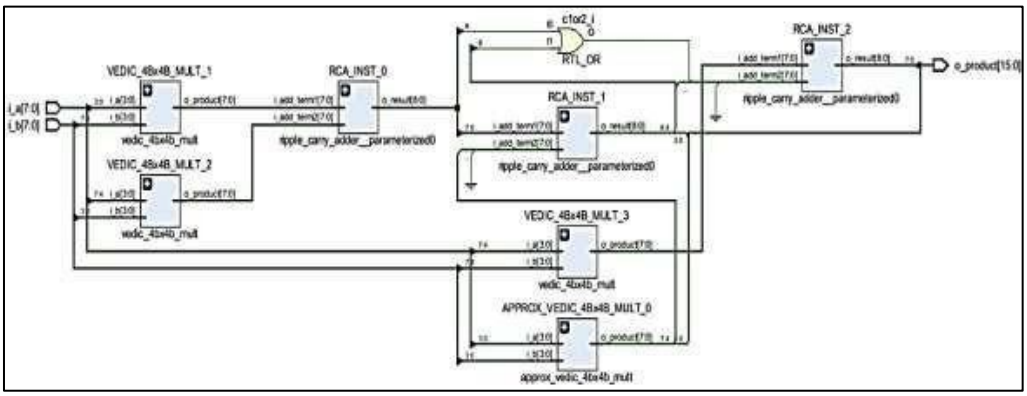


Figure.10 RTL Schematic Exact 8x8 Approx Vedic Multiplier

| Site Type | Used | Fixed | Available | Util% |
|---|---|---|---|---|
| Slice LUTs* | 103 | 0 | 14400 | 0.72 |
| LUT as Logic | 103 | 0 | 14400 | 0.72 |
| LUT as Memory | 0 | 0 | 6000 | 0.00 |
| Slice Registers | 0 | 0 | 28800 | 0.00 |
| Register as Flip Flop | 0 | 0 | 28800 | 0.00 |
| Register as Latch | 0 | 0 | 28800 | 0.00 |
| F7 Muxes | 0 | 0 | 8800 | 0.00 |
| F8 Muxes | 0 | 0 | 4400 | 0.00 |

Figure.11 Area Report 8x8 AVM

```
Max Delay Paths
--------------------------------------------------------------------------------
Slack:                  inf
  Source:               i_b[4]
                          (input port)
  Destination:          o_product[15]
                          (output port)
  Path Group:           (none)
  Path Type:            Max at Slow Process Corner
  Data Path Delay:      9.590ns  (logic 4.030ns (42.022%)  route 5.560ns (57.978%))
  Logic Levels:         9  (IBUF=1 LUT3=1 LUT5=2 LUT6=4 OBUF=1)
```

Figure.12 Max Delay Path 8x8 AVM

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Figure.13 Power status

## ADVANTAGES

- **Energy Efficiency**

  The use of approximate computing reduces power consumption, making it ideal for battery-powered devices such as smartphones, IoT devices, and embedded systems.

  Lower energy requirements contribute to longer battery life in portable applications.

- **High-Speed Computation**

  Approximate multipliers typically require fewer logic gates and shorter critical paths, leading to reduced computation time and faster processing speeds. Enables real-time image processing in applications like video streaming, medical imaging, and autonomous systems.

- **Reduced Hardware Complexity**

  By using approximate multiplication techniques, the circuit complexity is significantly reduced compared to traditional exact multipliers.

  Requires fewer transistors, leading to smaller chip area and cost savings in hardware manufacturing.

- **Acceptable Image Quality Trade-offs**

  Many image processing applications (e.g., object detection, facial recognition, and edge detection) do not require fully precise calculations, making approximate multipliers an effective solution.

  The small amount of error introduced does not significantly degrade the overall image quality.

- **Improved Performance in Machine Learning & AI**

  Neural networks and deep learning models often operate on approximate computations. Using hybrid approximate multipliers in AI accelerators can reduce power consumption without significantly affecting accuracy.

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## APPLICATIONS

- **Image & Video Processing:**

  Used in real-time video streaming, where fast image computations are needed with minimal energy consumption.

  Suitable for video compression algorithms like JPEG, MPEG, and HEVC to reduce computational complexity.

  Can be applied in image filtering, edge detection, and feature extraction in computer vision applications.

- **Machine Learning & AI Accelerators:**

  Helps in deep learning inference for image classification and object detection while reducing power consumption.

  Used in AI-powered facial recognition and gesture recognition systems in smart devices.

  Optimizes neural network processing by speeding up matrix multiplications.

- **Medical Image Processing:**

  Used in X-ray, MRI, and CT scan processing to enhance medical images while maintaining energy efficiency.

  Helps in pattern recognition for disease detection, such as identifying tumors in medical scans.

  Assists in biomedical signal processing, like ECG and EEG analysis.

- **Augmented Reality (AR) & Virtual Reality (VR):**

  Used in real-time AR/VR rendering, where energy-efficient processing is needed for smooth user experiences.

  Enhances gesture tracking and motion detection in immersive environments.

- **Mobile and Embedded Systems:**

  Useful in smartphones, tablets, and wearable for camera image processing, face unlocking, and video encoding.

  Helps optimize augmented reality applications in mobile devices without draining the battery.

## CONCLUSION

The efficiency of VLSI circuit design is primarily determined by three key factors: area, power consumption, and delay. Traditional multiplication architectures often face challenges in optimizing these parameters simultaneously. In contrast, the proposed Hybrid Approximate Vedic Multiplier (HAVM) presents a novel approach that significantly enhances computational efficiency while minimizing power consumption and hardware

complexity.

By leveraging the Urdhva Tiryagbhyam sutra of Vedic Mathematics, the proposed HAVM generates partial products in parallel, thereby eliminating redundant multiplication steps and accelerating the multiplication process. This results in a faster and more power- efficient computation compared to conventional multipliers. Additionally, the HAVM's two- stage operation, which includes partial product generation followed by approximate addition using NAND-based Half Adders (NHA) and Ripple Carry Adders (RCA), further reduces the overall computational burden.

One of the most significant advantages of this architecture is its ability to lower power consumption and area requirements while maintaining acceptable accuracy for specific applications. By reducing the number of half adders and full adders, the HAVM achieves an optimal balance between hardware efficiency and computational speed. This makes it highly suitable for energy-constrained environments, such as real-time image and signal processing applications, where slight inaccuracies are tolerable.

Compared to traditional multipliers, the proposed 8-bit HAVM demonstrates superior energy efficiency, making it an ideal choice for low-power, high-speed applications. The integration of NHA cells in the Vedic architecture further enhances power optimization and reduces latency. Given its design advantages, the HAVM is particularly well-suited for DSP applications, embedded systems, and AI-driven computing, where speed and power efficiency are prioritized over absolute precision.

## FUTURE SCOPE

**1.Enhanced Energy Efficiency:**

- The demand for low-power computing, particularly in mobile devices, IoT, and edge computing, is growing. Improving the energy efficiency of image processing algorithms using hybrid approximate multipliers could result in substantial power savings, especially for real-time applications.

**2.AI and Machine Learning Integration:**

- Combining approximate multipliers with machine learning models could lead to faster processing with lower power consumption. As AI increasingly relies on image data (e.g., in computer vision and object recognition), leveraging hybrid approximate multipliers could optimize both training and inference phases in AI systems.

**REFERENCES**

1. G. Ganesh Kumar and V. Charishma, "Design of High Speed Vedic Multiplier using Vedic Mathematics Techniques," International Journal of Scientific and Research Publications, vol. 2, no. 3,
2. pp. 1-5, 2012.
3. P. Verma and K. K. Mehta, "Implementation of an Efficient Multiplier based on Vedic Mathematics Using EDA Tool," International Journal of Engineering and Advanced Technology, vol. 1, no. 5, pp. 75-79, 2012.

4. M. Ramalatha, K. D. Dayalan, P. Dharani, and S. Deoborah, "High Speed Energy Efficient ALU Design using Vedic Multiplication Techniques," International Conference on Advances in Computational Tools for Engineering Applications, pp. 600-603, 2009.
   A. M. Shamsuddin, M. F. Ain, and M. H. M. Yusof, "Design and Implementation of 8- bit Vedic Multiplier using VHDL," International Journal of Computer Applications, vol. 63, no. 16, pp. 975- 8887, 2013.
5. S. S. Kerur, P. R. Arjun, R. S. Balaji, and S. G. Vijaya, "Implementation of Vedic Multiplier for Digital Signal Processing," International Journal of Computer Applications, vol. 19, no. 6, pp. 975-8887, 2011.
6. P. Soni and P. K. Jain, "Design and Implementation of Low Power Multiplier using Vedic Multiplication Technique," International Journal of Computer Science and Mobile Computing, vol. 3, no. 5, pp. 1281-1286, 2014.
7. R. Sridevi, A. Palakurthi, A. Sadhula, and H. Mahreen, "Design of a High Speed Multiplier (Ancient Vedic Mathematics Approach)," International Journal of Engineering Research and Applications, vol. 2, no. 3, pp. 383-386, 2012.
8. P. Mehta and D. Gawali, "Conventional versus Vedic Mathematical Method for Hardware Implementation of a Multiplier," International Conference on Advances in Computing, Control, and Telecommunication Technologies, pp. 640-642, 2009.
9. K. Singh and R. S. Gohil, "Design and Implementation of 32-bit Vedic Multiplier," International Journal of Engineering Research and Applications, vol. 4, no. 1, pp. 117- 120, 2014.